

Claims

- 1 1. A method of impedance control, comprising:
  - 2
  - 3 providing an input/output cell having a controllable input/output impedance;
  - 4
  - 5 providing a reference cell including a node having a variable voltage;
  - 6
  - 7 comparing the voltage of the node to a reference voltage;
  - 8
  - 9 adjusting the voltage of the node during a defined period and according to a defined
  - 10 procedure;
  - 11
  - 12 during said defined period, generating a digital signal; and
  - 13
  - 14 transmitting the digital signal to the input/output cell to adjust the input/output
  - 15 impedance.
- 1 2. A method according to Claim 1, wherein:
  - 2
  - 3 the generating step includes the step of increasing a count value during said defined
  - 4 period; and
  - 5
  - 6 the transmitting step includes the step of transmitting said count value to the input/output
  - 7 cell after the defined period.
- 1 3. A method according to Claim 2, wherein:
  - 2
  - 3 the reference cell includes a series of transistors for adjusting the voltage of the node;
  - 4 and
  - 5

6 the adjusting step includes the step of using the count value to activate said transistors in  
7 a given order to adjust the voltage of the node.

1 4. A method according to Claim 1, wherein:

2  
3 the reference cell includes a first set of transistors for adjusting the voltage of the node;

4  
5 the input/output cell includes a second set of transistors for adjusting the input/output  
6 impedance;

7  
8 each of the transistors of said first set is associated with one of the transistors in said  
9 second set;

10  
11 the adjusting step includes the step of activating a subset of the first set of transistors to  
12 adjust the voltage of said node; and

13  
14 the transmitting step includes the step of transmitting the digital signal to the  
15 input/output cell to activate transistors of the second set of transistors that are associated  
16 with said subset of the first set of transistors.

1 5. A method according to Claim 1, wherein:

2  
3 the input/output impedance of the input/output cell varies in a defined manner as a  
4 function of a given set of variables; and

5  
6 the variable voltage of the node of the reference cell also varies in said defined manner  
7 as a function of said given set of variables.

1 6. A method according to Claim 5, wherein:

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3 the reference cell includes a reference resistor for establishing the variable voltage at  
4 said node; and

5

6 said resistor has an impedance that varies in said defined manner as a function of said  
7 given set of variables.

1 7. A method according to Claim 1, wherein the adjusting step includes the steps of:

2

3 if the voltage of the node is less than the reference voltage, then increasing the voltage of  
4 the node in a first manner; and

5

6 if the voltage of the node is more than the reference voltage, then decreasing the voltage  
7 of the node in a second manner.

1 8. A method according to Claim 7, wherein:

2

3 the increasing step includes the steps of

4

5 i) applying a first signal to a digital controller, and

6

7 ii) the digital controller applying a signal to the reference cell to increase the voltage  
8 of the node;

9

10 the decreasing step includes the steps of

11

12 i) applying a second signal to the digital controller, and

13

14 ii) the digital controller applying a signal to the reference cell to decrease the  
15 voltage of the node; and

16

17 the generating step includes the step of using the digital controller to generate the digital  
18 signal.

1 9. A circuit for controlling the impedance of an input/output cell having a varying  
2 input/output impedance, said circuit comprising:

3

4

5 a node having a variable voltage;

6

7 a comparator for comparing the voltage of the node to a reference voltage;

8

9 means for adjusting the voltage of the node during a defined period and according to a  
10 defined procedure;

11

12 a digital generator for generating a digital signal during said defined period; and

13

14 means for transmitting the digital signal to the input/output cell to adjust the input/output  
15 impedance.

1 10. A circuit according to Claim 9, wherein:

2

3 the digital generator increases a count value during said defined period; and

4

5 the transmitting means transmits said count value to the input/output cell after the  
6 defined period.

1 11. A circuit according to Claim 10, wherein the adjusting means includes:

2

3 a series of transistors for adjusting the voltage of the node; and

4

5 means for using the count value to activate said transistors in a given order to adjust the  
6 voltage of the node.

1 12. A circuit according to Claim 9, wherein:

2  
3 the input/output cell includes a first set of transistors for adjusting the input/output  
4 impedance;

5  
6 the circuit further includes a second set of transistors for adjusting the voltage of the  
7 node;

8  
9 each of the transistors of said second set is associated with one of the transistors in said  
10 first set;

11  
12 the adjusting means includes means for activating a subset of the second set of  
13 transistors to adjust the voltage of said node; and

14  
15 the transmitting means includes means for transmitting the digital signal to the  
16 input/output cell to activate transistors of the first set of transistors that are associated  
17 with said subset of the second set of transistors.

1 13. A circuit according to Claim 9, wherein:

2  
3 the input/output impedance of the input/output cell varies in a defined manner as a  
4 function of a given set of variables; and

5  
6 the variable voltage of said node also varies in said defined manner as a function of said  
7 given set of variables.

1 14. A circuit according to Claim 13, wherein:

2 the circuit further includes a reference resistor for establishing the variable voltage at  
3 said node; and

4

5 said resistor has an impedance that varies in said defined manner as a function of said  
6 given set of variables.

1 15. A circuit according to Claim 9, wherein the adjusting means includes:

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3 means for increasing the voltage of the node in a first manner if the voltage of the node  
4 is less than the reference voltage; and

5

6 means for decreasing the voltage of the node in a second manner if the voltage of the  
7 node is more than the reference voltage.

1 16. A circuit according to Claim 9, wherein said circuit is a digital controller

2 designed as a synthesized core or macro.